IN THE CLAIMS

What is claimed is:

1. A semiconductor device having a first operational mode, comprising:

a reference configuration circuit providing a first and second reference potential, the reference configuration circuit including

a bond pad for receiving an external potential to be used as the second reference potential in the first operational mode;

a test mode of operation in which the bond pad receives an external potential to be used as the first reference potential.

2. The semiconductor device according to claim 1, wherein:

the reference configuration circuit includes a second reference potential generator receiving the first reference potential and providing the second reference potential in the test mode.

3. The semiconductor device according to claim 1, wherein:

the second reference potential is an input buffer reference potential.

4. The semiconductor device according to claim 1 is programmably configured to operate in the first operational mode or a second operational mode.

5. The semiconductor device according to claim 4, wherein:

the reference configuration circuit includes a second reference potential generator receiving the first reference potential;

in normal operation, when the semiconductor device is configured to operate in the first operational mode, the first reference potential is generated by a first reference potential generator; and

when the semiconductor device is configured to operate in the second operational mode, the second reference potential is generated by the second reference potential generator.

6. The semiconductor device according to claim 5, wherein:

in the test mode of operation, the second reference potential is generated by the second reference potential generator.

7. The semiconductor device according to claim 1, wherein the reference configuration circuit includes a fuse that is intact in the test mode of operation and blown in the first operational mode.

8. A semiconductor device having a first operating mode, comprising:

a reference configuration circuit, including

a bond pad;

a control circuit providing a first control signal having a first logic level in a normal operation and a second logic level in a test

operation; and

a reference selection circuit coupled to receive the control signal and provide a first reference potential at a first node and a second reference potential at a second node;

wherein in the normal operation, the selection circuit provides a potential received on the bond pad to the second node and in the test operation the selection circuit provides the potential received on the bond pad to the first node.

9. The semiconductor device according to claim 8, wherein:

the control circuit includes a programmable device having a first state in the test operation and a second state in the normal operation.

10. The semiconductor device according to claim 8, wherein:

the reference selection circuit includes a first switch including a voltage translator coupled to receive the first control signal and provide a switch control output coupled to a control gate of a controllable impedance device having a controllable impedance path coupled between the bond pad and the first node.

11. The semiconductor device according to claim 8, wherein the reference configuration circuit further includes:

a reference potential generation circuit coupled to the reference

selection circuit; and

the reference selection circuit includes a second switch coupled to receive the first control signal and provide a low impedance path between the reference potential generation circuit and the first node when the first control signal has the first logic level and a high impedance path between the reference potential generation circuit and the first node when the first control signal has the second logic level.

12. The semiconductor device according to claim 8, wherein the reference configuration circuit further includes:

a second reference potential generation circuit coupled to the reference selection circuit; and

the reference selection circuit includes a third switch coupled to receive the first control signal and provide a low impedance path between the second reference potential generation circuit and the second node when the first control signal has the second logic level and a high impedance path between the reference potential generation circuit and the second node when the first control signal has the first logic level.

13. The semiconductor device according to claim 8, wherein:

the second reference potential generation circuit is coupled to receive the first reference potential and generate a potential that is proportional to the first reference potential.

14. The semiconductor device according to claim 8, wherein the control circuit is coupled to receive a power-up signal that forces the first control signal to the second logic level during power-up.

15. A semiconductor device programmably configured to operate in a first operational mode having first input signal specifications or a second operational mode having second input signal specifications, comprising:

a reference configuration circuit providing a first and second reference potential, the reference configuration circuit including

a bond pad for receiving an external potential to be used as the second reference potential in the first operational mode;

a test mode of operation in which the bond pad receives an external potential to be used as the first reference potential.

16. The semiconductor device according to claim 15, wherein:

the reference configuration circuit includes a second reference potential generator;

in normal operation, when the semiconductor device is configured to operate in the first operational mode the first reference potential is generated by a first reference potential generator; and

when the semiconductor device is configured to operate in the second operational mode, the second reference potential is generated by the second reference potential generator.

17. The semiconductor device according to claim 16, wherein the second reference potential is used as an input buffer reference potential.

18. The semiconductor device according to claim 15, including:

the reference configuration circuit includes a first reference potential generation circuit providing the first reference potential in a normal operation for both the first and second operational modes; and

the first reference generation circuit includes at least one programmable device for adjusting the potential provided.

19. The semiconductor device according to claim 15, further including:

a voltage-down circuit coupled to receive the first reference potential and generate an internal supply potential having a potential less than the first reference potential.

20. The semiconductor device according to claim 15 is a semiconductor memory device and the first operational mode is a SSTL mode and the second operational mode is a LVTTL mode.